FIG. 1

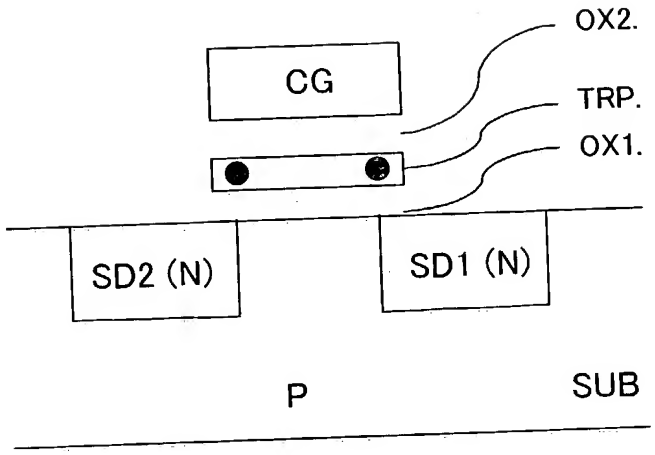
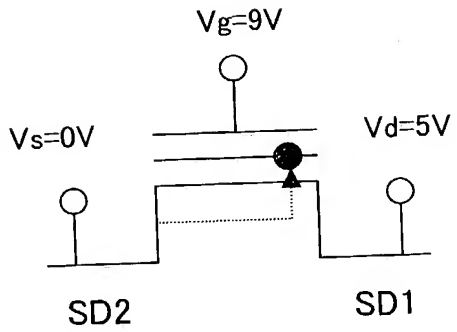
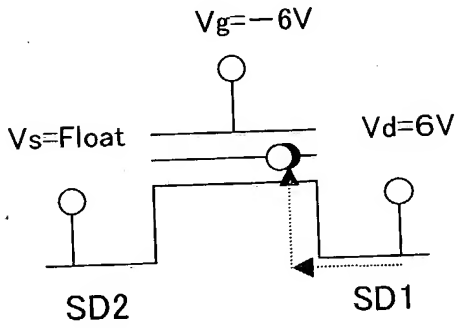


FIG. 2

A. WRITE OPERATION



B. ERASE OPERATION



C. READ-OUT OPERATION

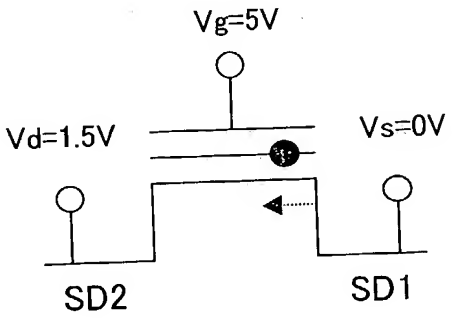


FIG. 3

PRIOR ART

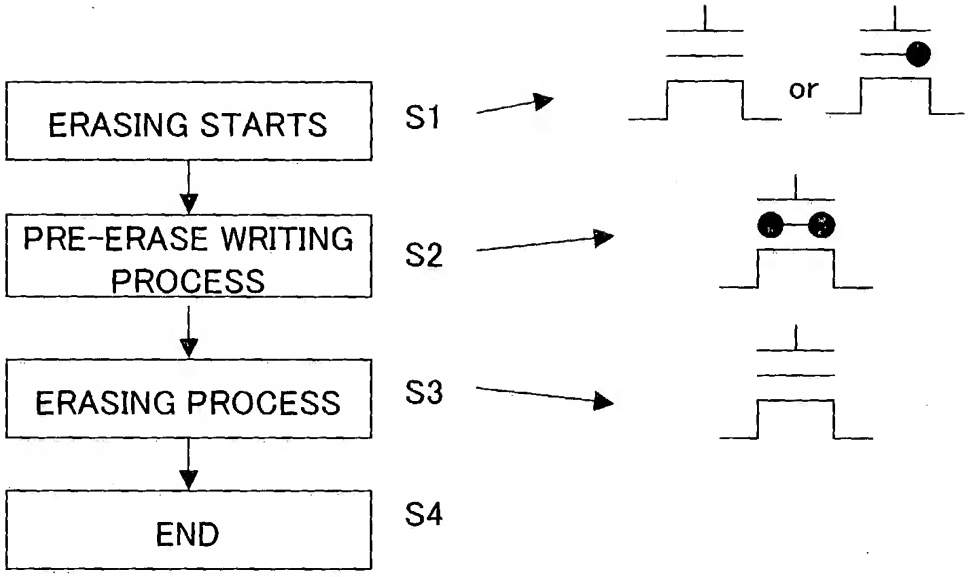


FIG. 4

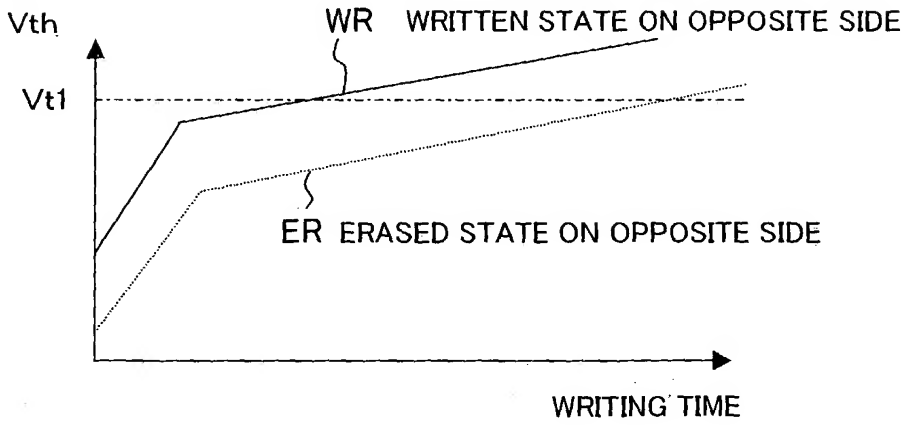


FIG. 5

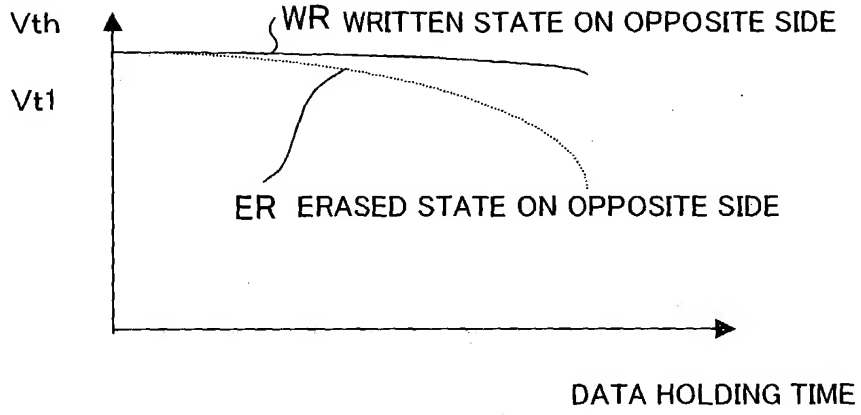

Vth
Vt1
WR WRITTEN STATE ON OPPOSITE SIDE
ER ERASED STATE ON OPPOSITE SIDE
DATA HOLDING TIME

FIG. 6

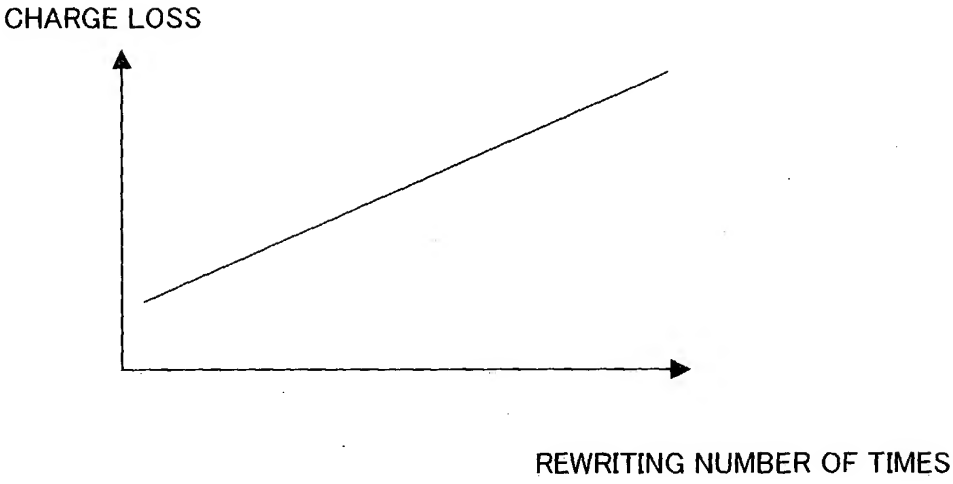

CHARGE LOSS
REWRITING NUMBER OF TIMES

FIG. 7

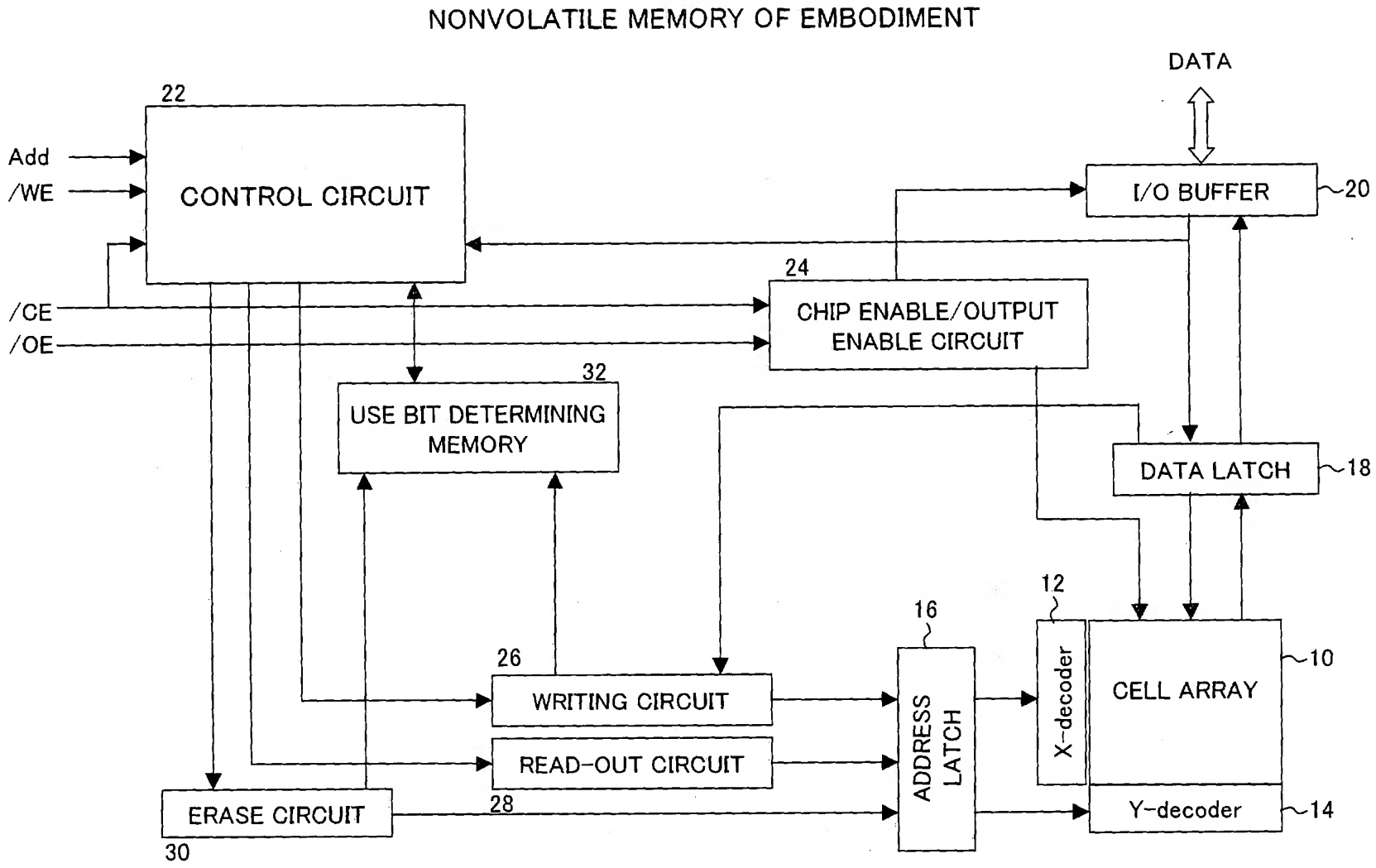

NONVOLATILE MEMORY OF EMBODIMENT
DATA
22
Add
/WE
CONTROL CIRCUIT
I/O BUFFER
20
24
/CE
/OE
CHIP ENABLE/OUTPUT ENABLE CIRCUIT
32
USE BIT DETERMINING MEMORY
DATA LATCH
18
12
16
26
WRITING CIRCUIT
ADDRESS LATCH
X-decoder
CELL ARRAY
10
READ-OUT CIRCUIT
ERASE CIRCUIT
28
Y-decoder
14
30

FIG. 8

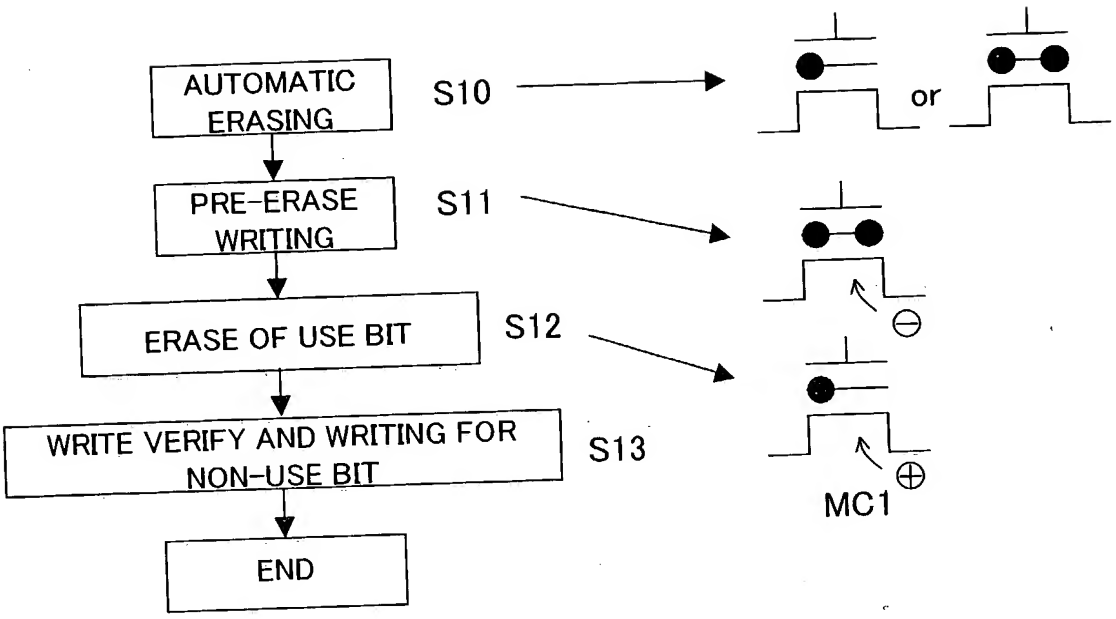

AUTOMATIC ERASING
S10
or
PRE-ERASE WRITING
S11
ERASE OF USE BIT
S12
WRITE VERIFY AND WRITING FOR NON-USE BIT
S13
MC1
END

FIG. 9

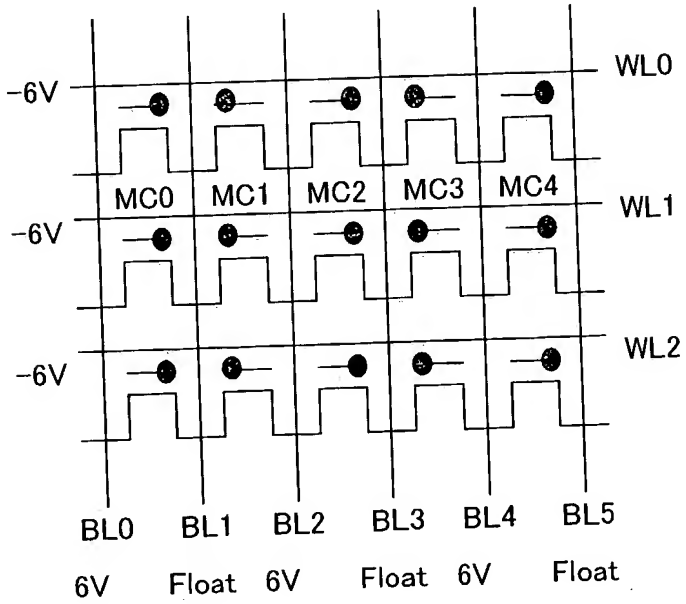

WL0
-6V
MC0
MC1
MC2
MC3
MC4
WL1
-6V
WL2
-6V
BL0
BL1
BL2
BL3
BL4
BL5
6V
Float
6V
Float
6V
Float

FIG. 10

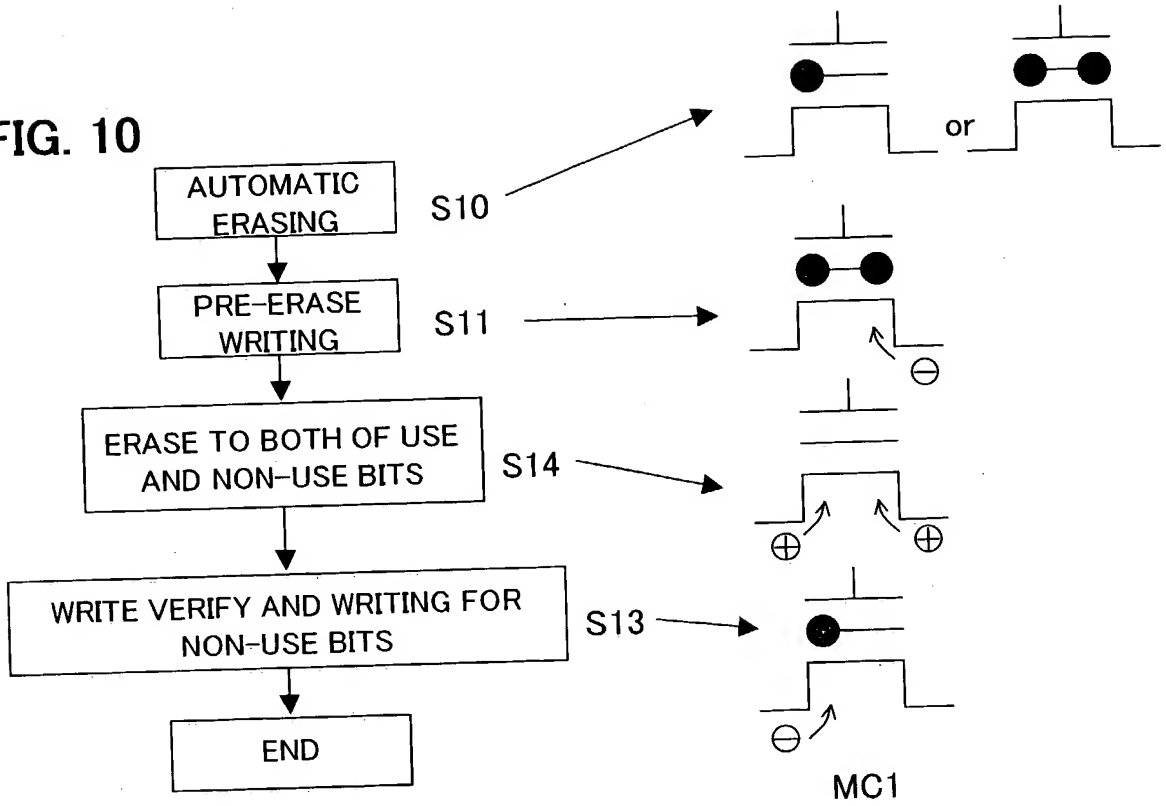

AUTOMATIC ERASING
S10
or
PRE-ERASE WRITING
S11
ERASE TO BOTH OF USE AND NON-USE BITS
S14
WRITE VERIFY AND WRITING FOR NON-USE BITS
S13
END
MC1

FIG. 11

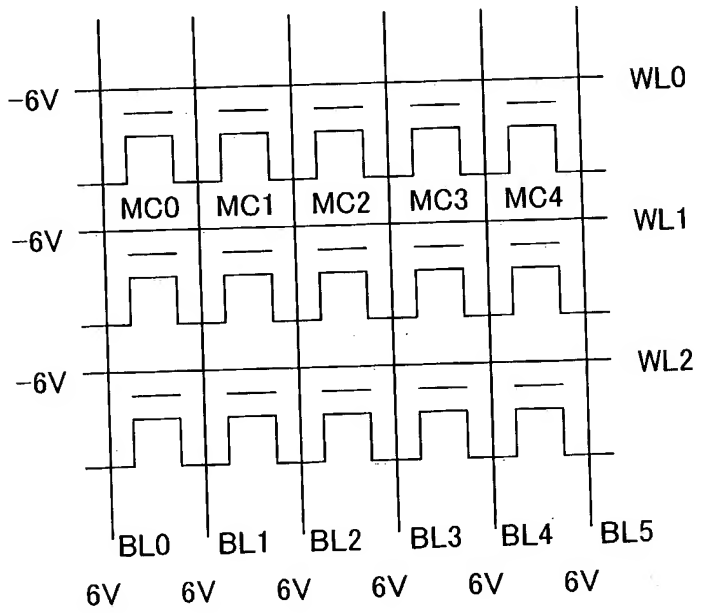

WL0
-6V
MC0
MC1
MC2
MC3
MC4
WL1
-6V
WL2
-6V
BL0
BL1
BL2
BL3
BL4
BL5
6V
6V
6V
6V
6V
6V

FIG. 12

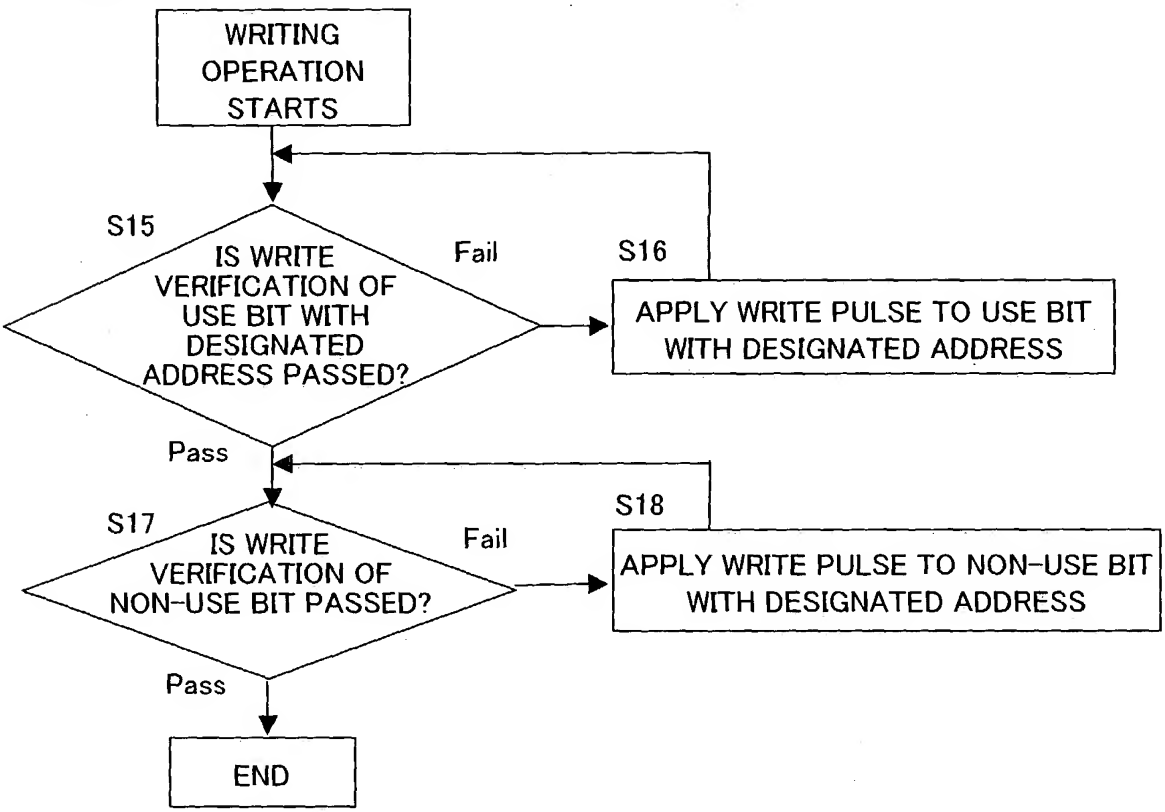

WRITING OPERATION STARTS
S15
IS WRITE VERIFICATION OF USE BIT WITH DESIGNATED ADDRESS PASSED?
Fail
S16
APPLY WRITE PULSE TO USE BIT WITH DESIGNATED ADDRESS
Pass
S17
IS WRITE VERIFICATION OF NON-USE BIT PASSED?
Fail
S18
APPLY WRITE PULSE TO NON-USE BIT WITH DESIGNATED ADDRESS
Pass
END

FIG. 13

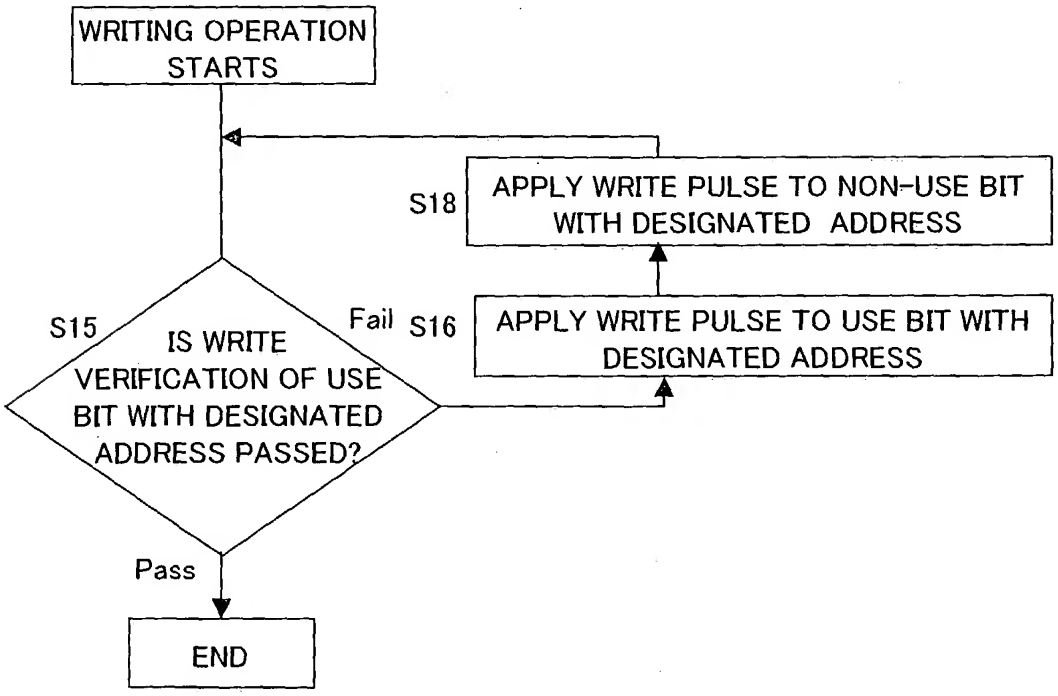

WRITING OPERATION STARTS
S18
APPLY WRITE PULSE TO NON-USE BIT WITH DESIGNATED ADDRESS
S15
IS WRITE VERIFICATION OF USE BIT WITH DESIGNATED ADDRESS PASSED?
Fail
S16
APPLY WRITE PULSE TO USE BIT WITH DESIGNATED ADDRESS
Pass
END

FIG. 14

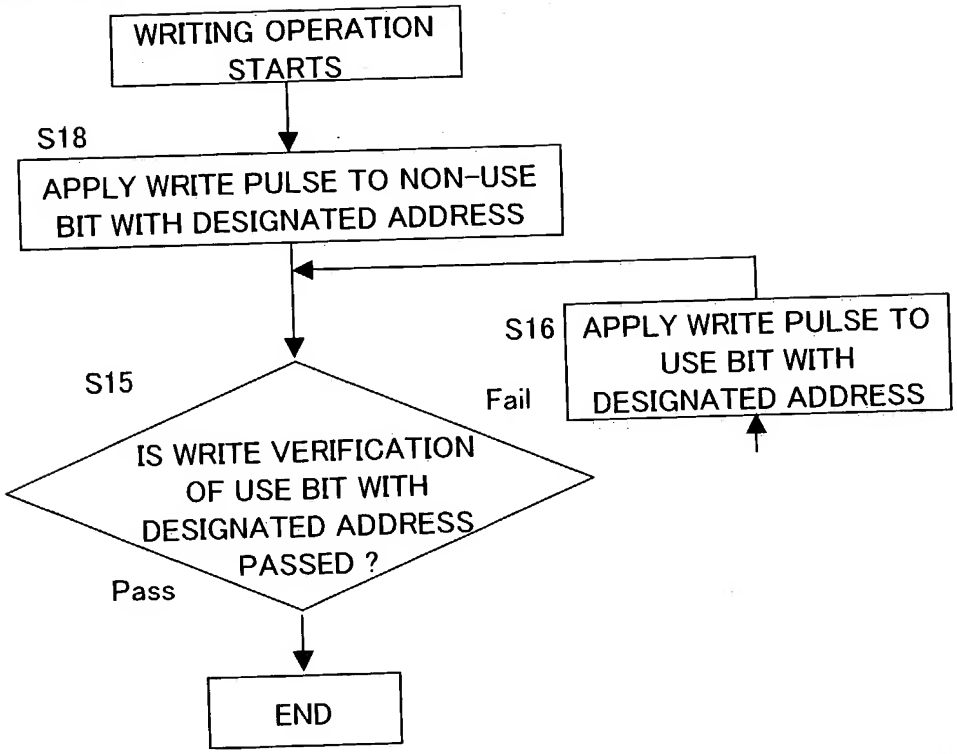

WRITING OPERATION STARTS
S18
APPLY WRITE PULSE TO NON-USE BIT WITH DESIGNATED ADDRESS
S16
APPLY WRITE PULSE TO USE BIT WITH DESIGNATED ADDRESS
Fail
S15
IS WRITE VERIFICATION OF USE BIT WITH DESIGNATED ADDRESS PASSED ?
Pass
END

FIG. 15

AUTOMATIC ERASING OPERATION (1) WITH REPLACEMENT OF NON-USE BIT TO USE BIT, IN WHICH NON-USE BIT IS KEPT IN WRITTEN CONDITION

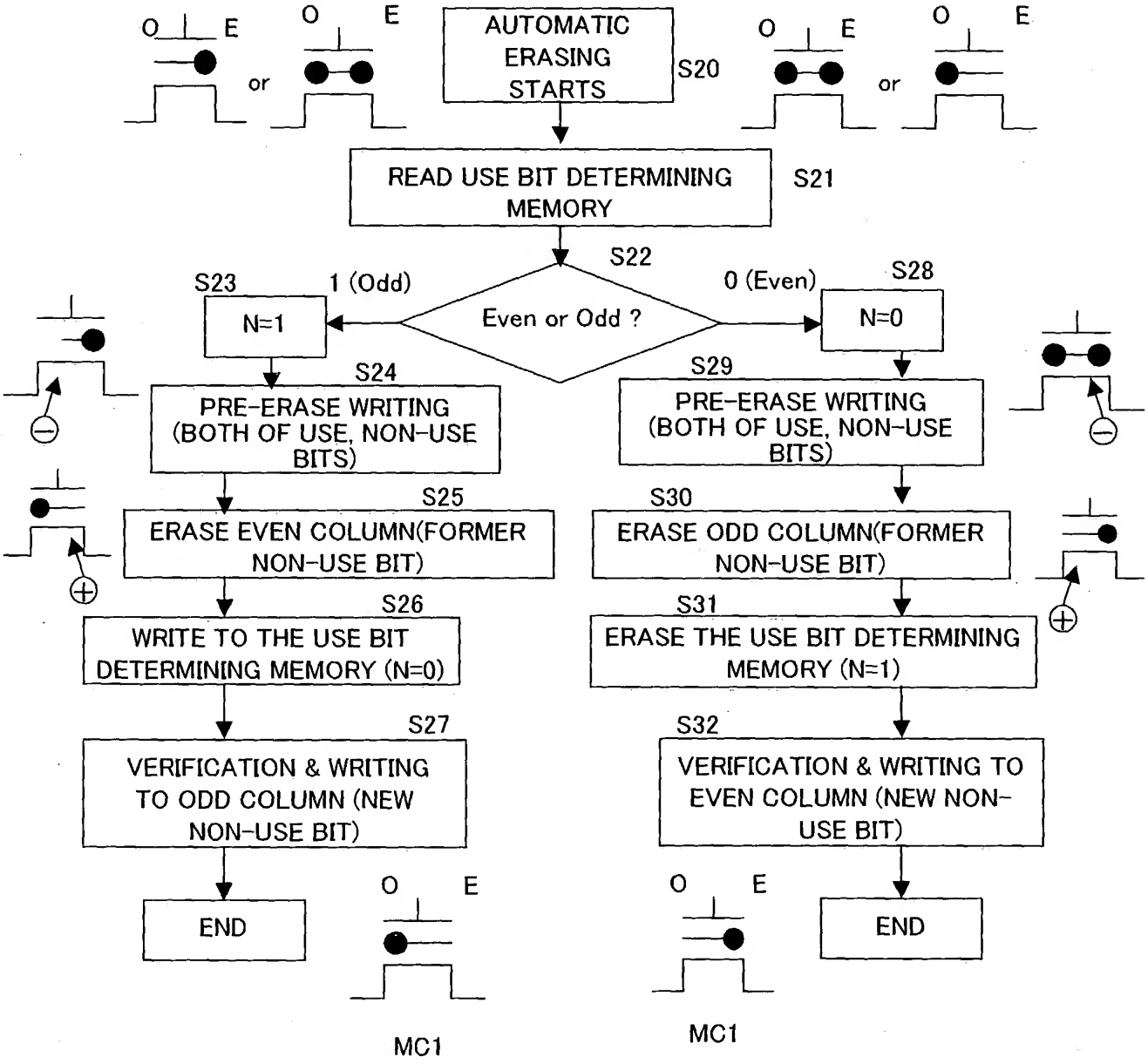


FIG. 16

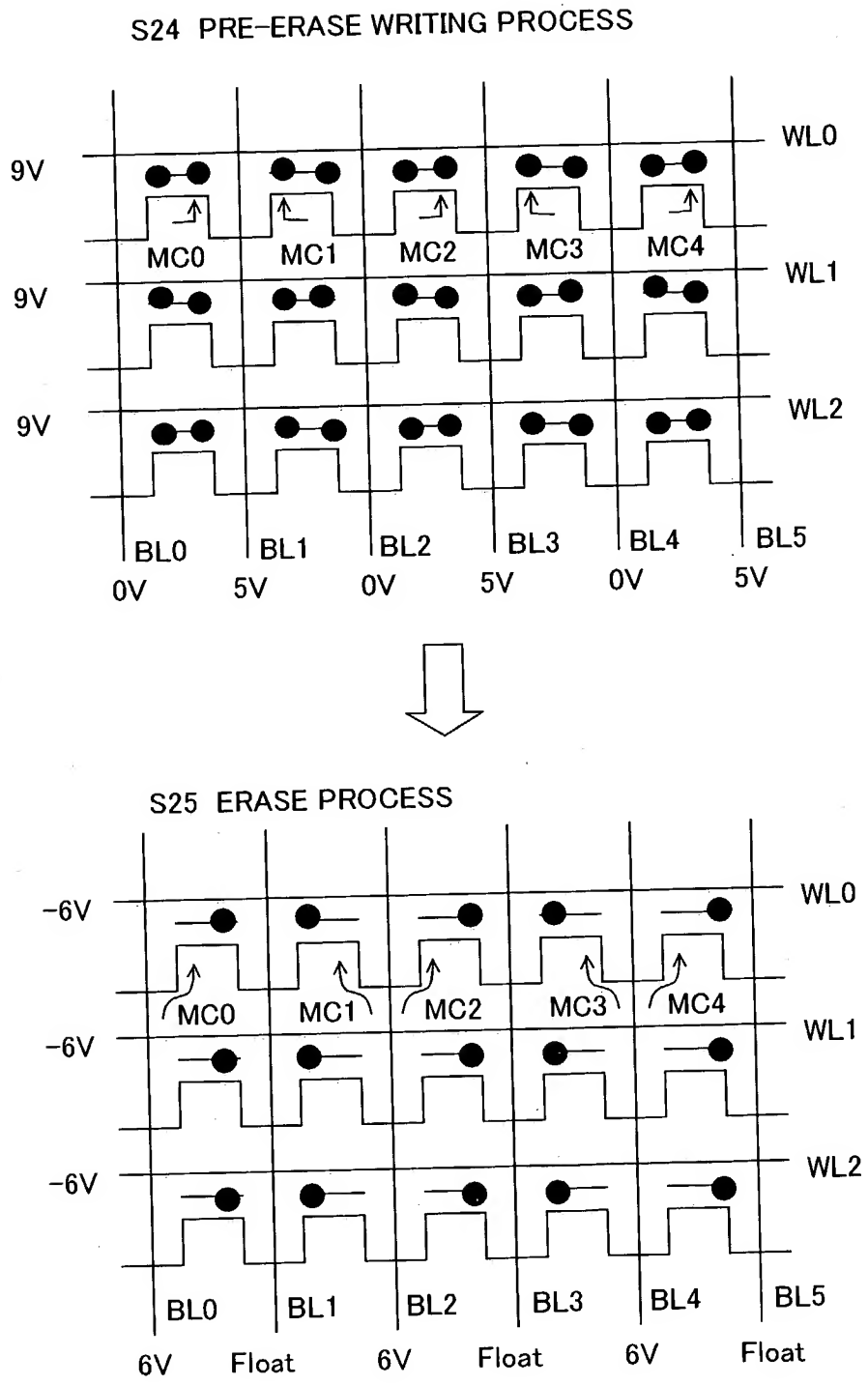

S24 PRE-ERASE WRITING PROCESS
9V
9V
9V
WL0
WL1
WL2
MC0
MC1
MC2
MC3
MC4
BL0
BL1
BL2
BL3
BL4
BL5
0V
5V
0V
5V
0V
5V
S25 ERASE PROCESS
-6V
-6V
-6V
WL0
WL1
WL2
MC0
MC1
MC2
MC3
MC4
BL0
BL1
BL2
BL3
BL4
BL5
6V
Float
6V
Float
6V
Float

FIG. 17

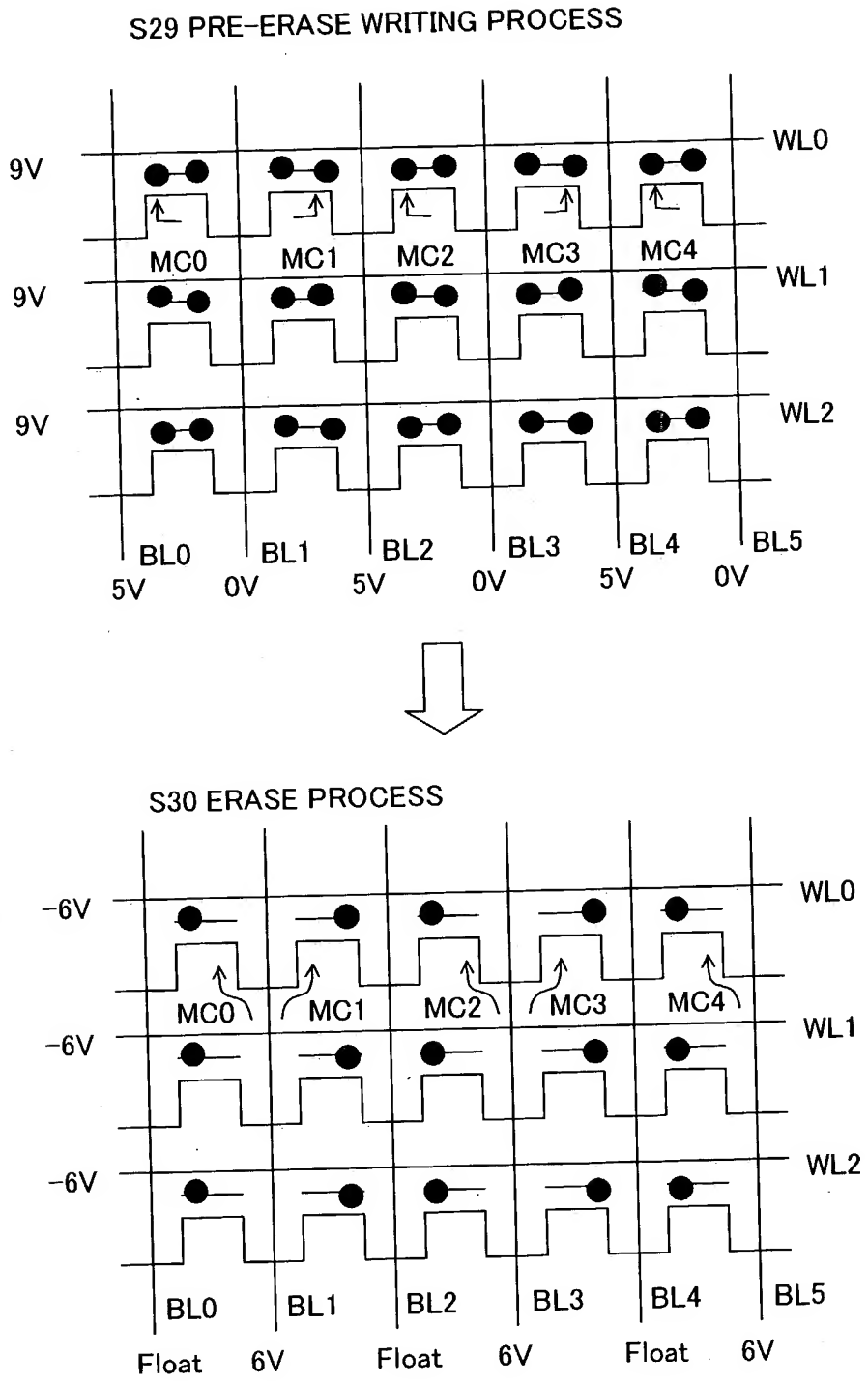

S29 PRE-ERASE WRITING PROCESS
9V
9V
9V
WL0
WL1
WL2
MC0
MC1
MC2
MC3
MC4
BL0
BL1
BL2
BL3
BL4
BL5
5V
0V
5V
0V
5V
0V
S30 ERASE PROCESS
-6V
-6V
-6V
WL0
WL1
WL2
MC0
MC1
MC2
MC3
MC4
BL0
BL1
BL2
BL3
BL4
BL5
Float
6V
Float
6V
Float
6V

FIG. 18

AUTOMATIC ERASING OPERATION (2) WITH REPLACEMENT OF NON-USE BIT TO USE BIT, IN WHICH NON-USE BIT IS KEPT IN WRITTEN CONDITION

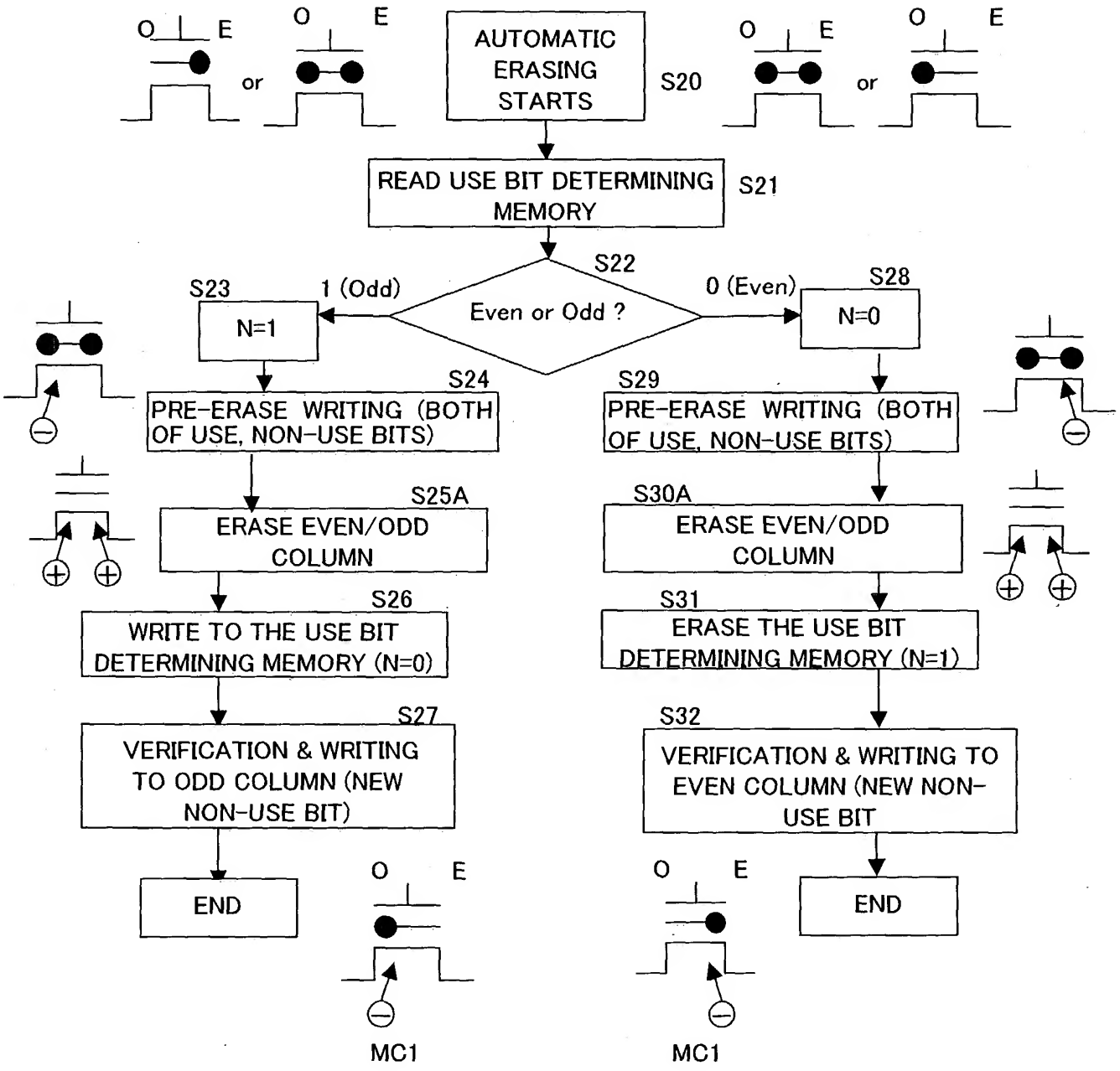


FIG. 19

AUTOMATIC ERASING OPERATION (3) WITH REPLACEMENT OF NON-USE BIT TO USE BIT, IN WHICH NON-USE BIT IS KEPT IN WRITTEN CONDITION

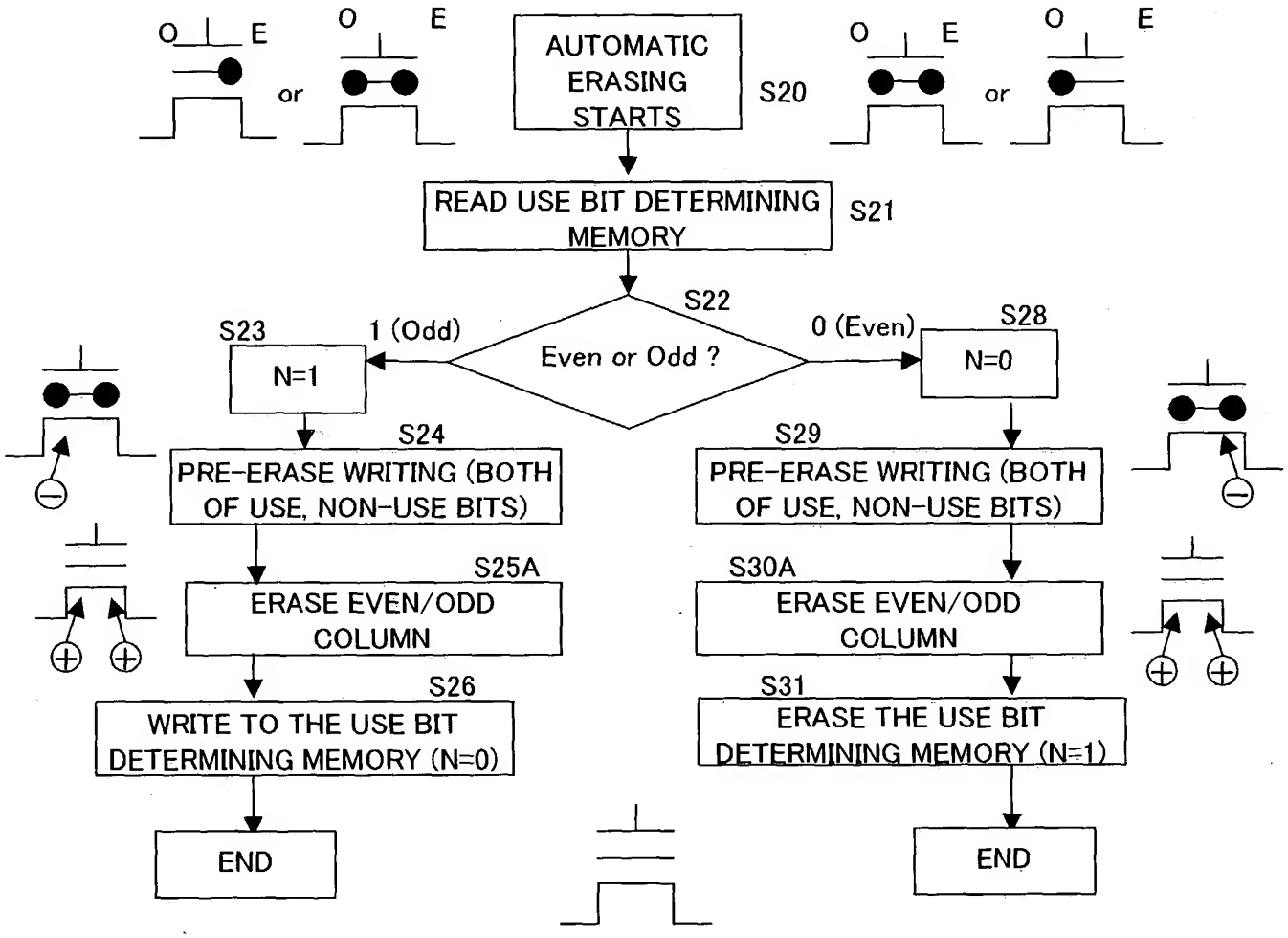


FIG. 20

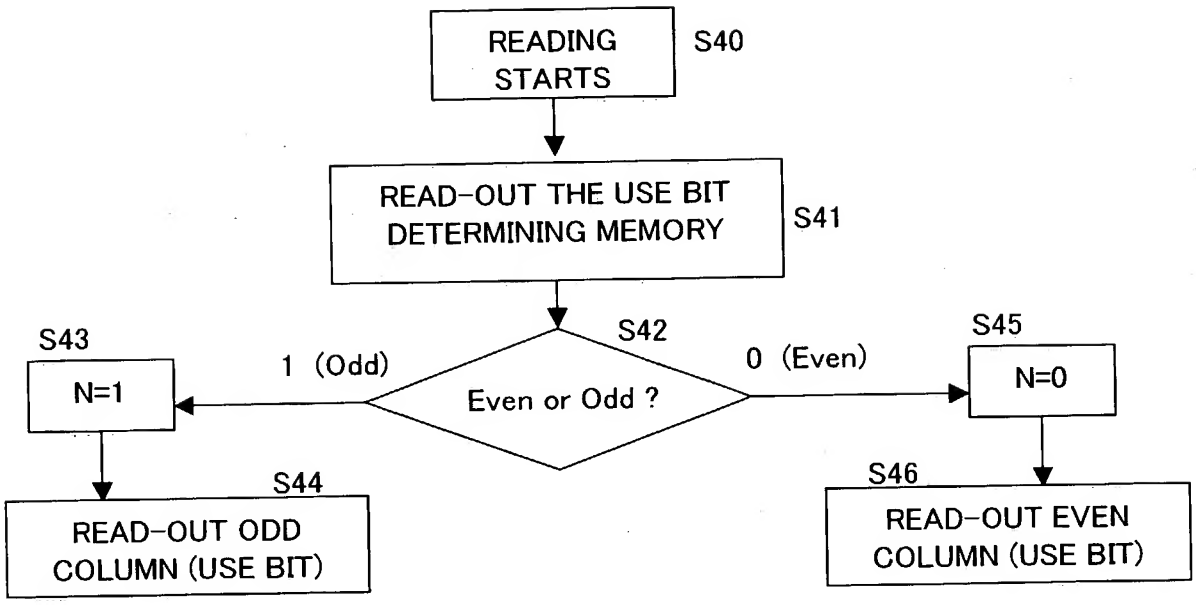

READING STARTS
S40
READ-OUT THE USE BIT DETERMINING MEMORY
S41
S42
Even or Odd ?
1 (Odd)
0 (Even)
S43
N=1
S44
READ-OUT ODD COLUMN (USE BIT)
S45
N=0
S46
READ-OUT EVEN COLUMN (USE BIT)

FIG. 21

AUTOMATIC ERASING OPERATION (1) WITH REPLACEMENT OF NON-USE BIT TO USE BIT, IN WHICH NON-USE BIT IS KEPT IN ERASED CONDITION

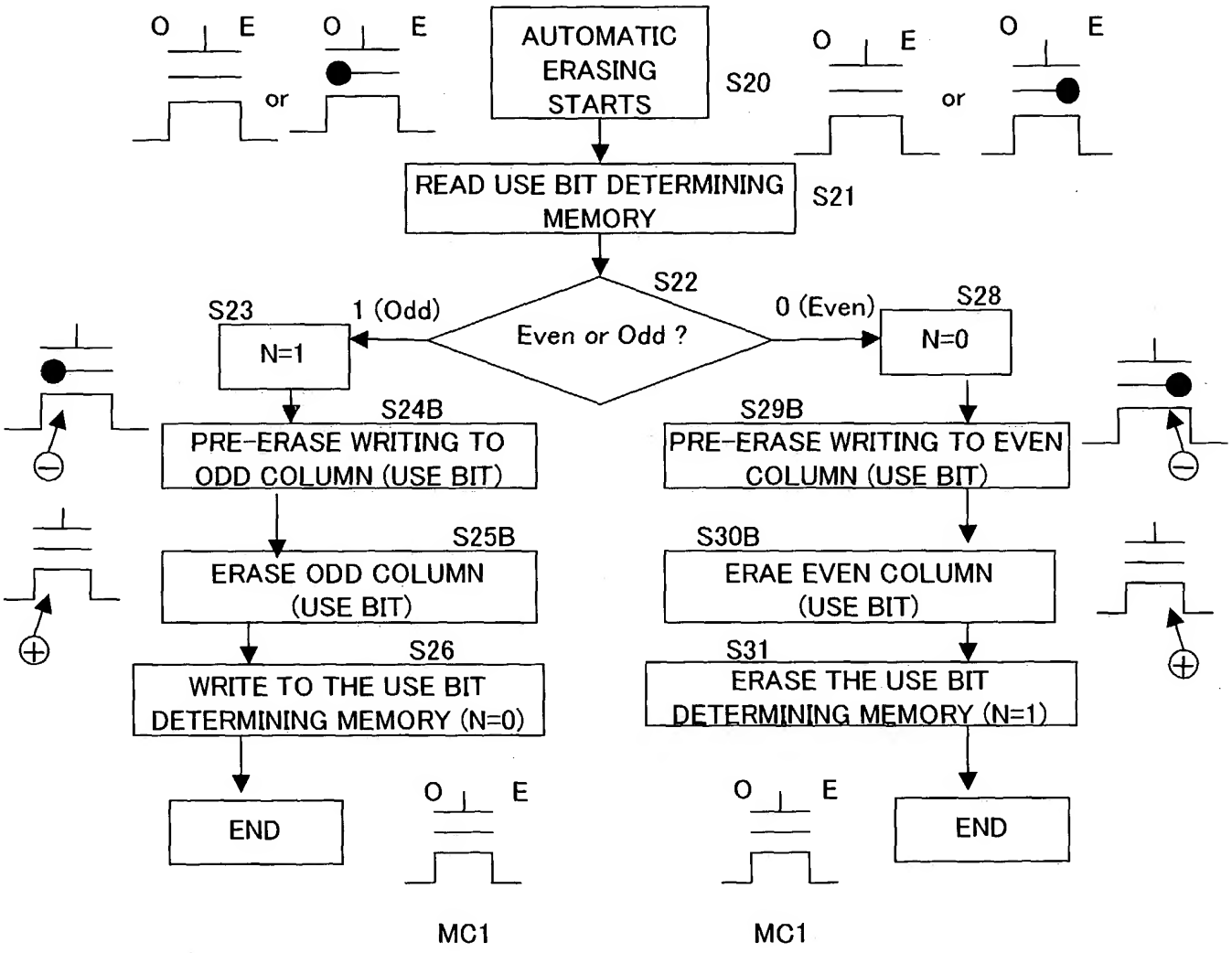


FIG. 22

AUTOMATIC ERASING OPERATION (2) WITH REPLACEMENT OF NON-USE BIT TO USE BIT, IN WHICH NON-USE BIT IS KEPT IN ERASED CONDITION